32-bit ARM Cortex-M0 MCU, 32KB Flash/4KB RAM, up to 30 fast I/O ports, 10 timers, 5 com. Interfaces, 1 ADC, 2 DACs, 3 ACMPs, 3 OPAs, 1 HALL_MID, 1.8 to 5.5V

Main Features

- **ARM® 32-bit Cortex®-M0 CPU Core**
  - 96 MHz maximum frequency
  - Single-cycle multiplication
  - Hardware division
- **Memories**
  - 32 Kbytes Flash (32-bit width), supporting prefetching and read / write protection
  - 4 Kbytes SRAM (32-bit width), dividing into two independent partitions (each 2 Kbytes)
- **Reset and power management**
  - 1.8V to 5.5V power supply and I/O
  - Two LDOs, one for low-power backup domains and one for core domains for system operation
  - POR_PDR
  - Low-voltage reset circuit (LVR): 8 reset points are available (1.6V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V, 3.5V, 4.0V)
  - Low-voltage detection circuit (LVD): 8 detection points are available (2.0V, 2.2V, 2.4V, 2.7V, 2.9V, 3.1V, 3.6V, 4.5V)
- **Clock System**
  - 4-to-20 MHz high-speed crystal oscillator (OSCH)
  - Internal 16 MHz factory-calibrated RC (RCH, 1% accuracy)
  - 32 kHz low-speed crystal oscillator (OSCL)
  - Internal 32 kHz factory-calibrated RC (RCL, 10% accuracy)
  - Internal maximum output 144MHz PLL, less than 100ps jitter
- **Low power**
  - Sleep, Stop, ULP Stop
- **Debug mode**
  - Serial wire debug port (SW-DP)
- **Boot modes**
  - Boot from Flash, SRAM or System Memory
- **Programming modes**
  - In-Circuit Serial Programming (ISP)
  - In Application Programming (IAP), including UART, I2C and SSP ports
- **Up to 30 fast I/O ports**
  - All I/Os mappable on 16 external interrupt vectors and almost all 5V tolerant
  - Supporting input floating, input pull-up input, input pull-down, output push-pull, output open-drain and output open-source
  - One or two analog channels for most IOs
  - I/O drive capability and slope are configurable in two levels
- **10 timers**
  - 1 x 16-bit advanced-control timer TIM1, 4 channels (with 3 complementary channels), supporting input capture/output comparison/PWM output/one-pulse output, quadrature (incremental) encoder input, dead-time control and emergency breaking
  - 1 x 16-bit general-purpose timer TIM3, 4 channels, supporting input capture/output comparison/PWM output/one-pulse output, and quadrature (incremental) encoder input
  - 1 x 16-bit general-purpose timer TIM14, 1 channel, supporting input capture/output comparison/PWM output/one-pulse output
  - 1 x 16-bit general-purpose timer TIM15, 2 channels (with 2 complementary channels), supporting input capture/output comparison/PWM output/one-pulse output, dead-time control and emergency braking

- 2 x 16-bit general-purpose timer TIM16/TIM17, 1 channel (with 1 complementary channel), supporting input capture/output comparison/PWM output/one-pulse output, dead-time control and emergency braking
- 1 independent watchdog timer
- 1 window watchdog timer
- SysTick timer: a 24-bit downcounter
- TIM1, TIM15, TIM16, and TIM17 support delay trigger and error-proof triggering mechanisms

- **Watch timer (WT)**
  - Supporting alarm clock and periodic wake-up
  - The buzz output with configurable frequencies
- **DMA**
  - 4 independent channels
  - Supported peripherals: SSP, I2C, UART, ADC, DAC, Timers
- **CRC calculation unit**
  - 8/16/32-bit configurable polynomials
- **Up to 5 communication interfaces**
  - 1 I2C interface (master/slave mode, 100K/400K/1Mbps rates, 7/10-bit addressing mode)
  - 2 UART interfaces (CTS/RTS hardware control, maximum baud rate of 4Mbps)
  - 2 SSP interfaces (master/slave mode, supporting Motorola SPI, TI SSI and National Semiconductor Microwire protocols, 4 to 16-bit frame size, up to 32Mbps)
- **1 x 12-bit A/D converter**
  - Conversion rate up to 1.5 MSPS
  - 18 channels (16 external channels and 2 internal channels)
  - Temperature sensor
  - Two separate sampling/hold circuits
  - Supporting internal and external reference voltages: 2.5V, 3.3V, 4V, 5V and VDDA
- **High-speed D/A converters and analog comparators**
  - 2 x 10-bit D/A converters with optional reference voltages 2.5V, 4V and VDDA
  - Hardware triggering and DMA transmission, supporting noise or triangular waveform generation
  - 3 analog comparators with reference voltages from DAC outputs, HALL_MID outputs, or external ports
- **3 operational amplifiers (OPA)**
  - Magnification: 1/2/4/6/10/16/20/32
- **Anti-electric force sampling (HALL_MID)**
  - 3 external voltage inputs sampling for motor control
- **Operating temperature**
  - Ambient temperature: -40°C to +125°C
  - Junction temperature: -40°C to +125°C
- **96-bit unique ID**

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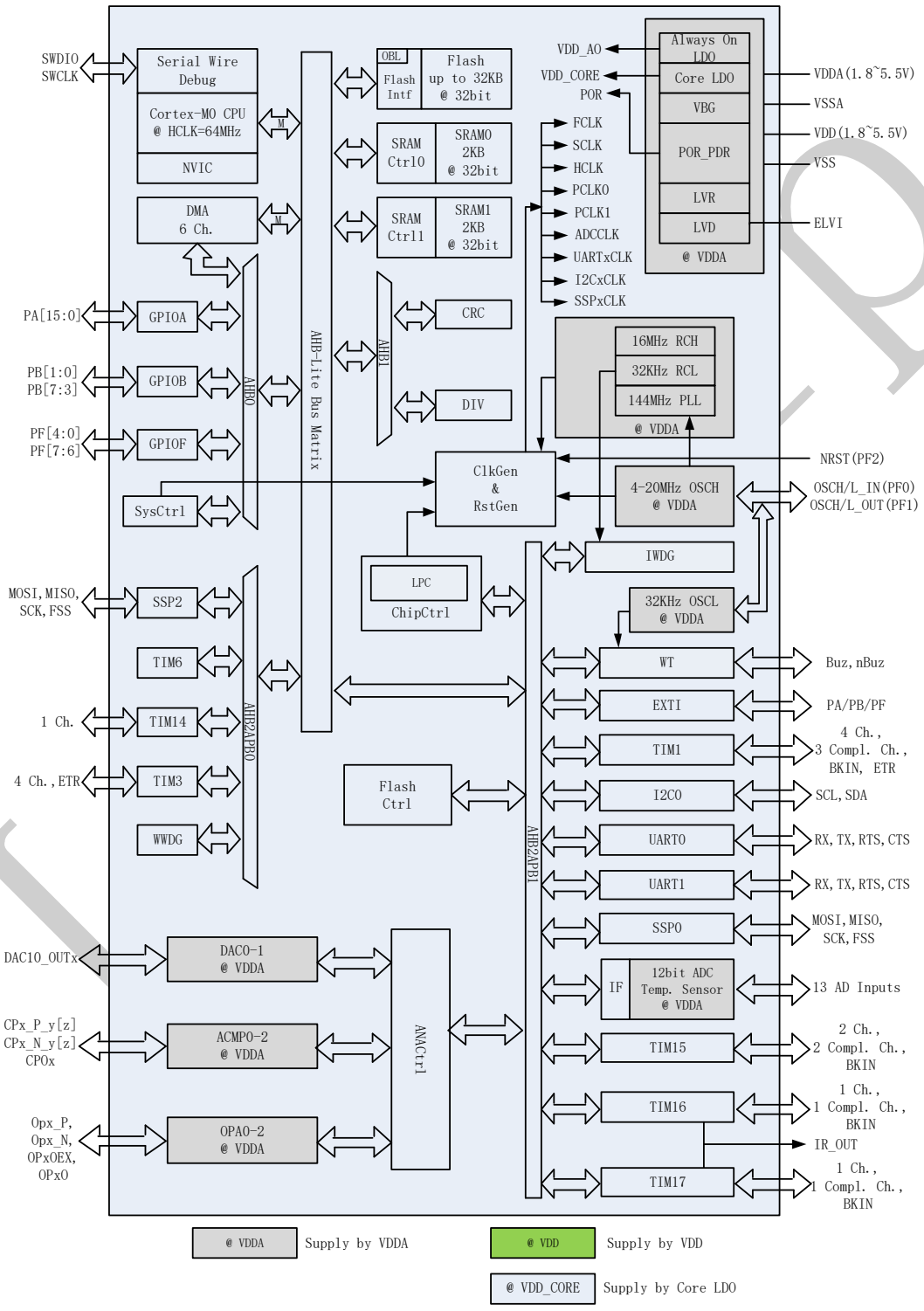
1. Function overview

1.1 General block diagram

Figure 1. LCM32F037 block diagram



1.2 32-bit processor core

The processor is a 32-bit embedded processor that provides a low-cost platform that meets the need of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance in the memory size usually associated with 8- and 16-bit devices.

The LCM32F037 products having a 32-bit CPU core, is compatible with all popular debugging tools and software on the market.

1.3 Embedded Flash

The LCM32F037 has an embedded 32K Flash for storing programs and data.

Flash access time depends on the CPU clock frequency: 0 wait cycles at CPU clock frequencies between 0 and 32MHz, 1 wait cycle at 32MHz to 64MHz, and 2 wait cycles at 64MHz or greater. In order to improve access efficiency and reduce waiting time, three 32-bit instruction prefetch buffers are realized.

Flash is functionally divided into three parts:

- **Main Memory** of 32 Kbytes, mainly used to store user programs and data
- 512 bytes **Option Bytes** for read/write protections and user configuration, etc.
- 1536 bytes **System Memory** for the boot loader, calibration information, device configuration, etc.

Write Protection prevents Main Memory from being tampered with a granularity of 1 Kbytes (2 Pages). There are 32 separate write protection regions in total.

Read protection contains three levels: Main Memory is divided into eight regions, each of which can be configured independently as read protection level 0 or 1; while read protection level 2 is used for all regions.

- Level 0: no readout protection.
- Level 1: memory readout protection. Flash cannot be read or written through the debug ports, programs in SRAM/System Memory, and programs in the Main Memory regions of read protection level 0.
- Level 2: chip readout protection. Debug function and the program function from SRAM/System Memory are prohibited.

1.4 Embedded SRAM

LCM32F037 contains two separate SRAM Banks that support simultaneous reading or writing. Each bank is 2 Kbytes (32-bit width) for a total of 4 Kbytes. The CPU can read or write to SRAM in 0 waiting cycles.

1.5 Boot modes

At startup, boot0pin and boot selector option bits are used to select one of three boot options:

- Boot from Main Memory
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Main Memory by using UART/I2C/SSP.

1.6 Power management

1.6.1 Power supply schemes

- VSS, VDD = 1.8 to 5.5V: external power supply for I/Os and the internal LDO regulators.
- VSSA, VDDA = 1.8 to 5.5V: external analog power supplies for the reset modules, RC oscillator, PLL and analog modules. The VDDA voltage must be greater than or equal to the VDD voltage and supplied before the VDD. VDDA and VSSA can be connected to VDD and VSS, respectively.

1.6.2 Power supply supervisor

LCM32F037 integrates a high-precision power-on reset (POR)/power-drop reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 1.8V. The device remains in reset mode when VDD is below a specified threshold, without an external reset circuit. It can then be powered off depending on the requirements of low-power applications.

LCM32F037 has an embedded programmable low voltage resetter (LVR) that monitors the VDD power supply and compares it to a specified threshold. The device is reset when the VDD is below the threshold voltage. The LVR default is on and can be turned off by software. LVR supports 8 low voltage reset points: 1.6V, 1.8V, 2.0V, 2.5V, 2.8V, 3.0V, 3.5V and 4.0V.

LCM32F037 also integrates a programmable low voltage detector (LVD) that monitors the VDD power supply and compares it to a specified threshold. An interrupt can be generated when VDD drops below the threshold and/or when VDD is higher than the threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. LVD default is off and needs to be turned on by software. LVD supports 8 voltage monitoring points: 2.0V, 2.2V, 2.4V, 2.7V, 2.9V, 3.1V, 3.6V and 4.5V.

1.6.3 LDO regulators

LCM32F037 contains two LDO regulators, one for backup power domain, and the other for kernel power domain. The LDOs are always enabled after reset. The kernel LDO is disabled in ultra-low power mode.

The kernel LDO has three operation modes:

- Main (MR), which has a drive capacity of three levels, is used in the normal mode
- Low power (LPR) is used in the Stop mode
- Power down (PD), is used for ultra-low power mode: the output of the LDO is in high impedance. In ultra-low power mode, the kernel circuitry is powered by the backup LDO (the contents of the registers and SRAM are maintained)

1.6.4 Low power modes

LCM32F037 supports three low-power modes to achieve a compromise between low power consumption, short startup time and available wakeup sources.

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. The kernel LDO keeps in the main mode.

- **Stop** mode

The Stop mode achieves quite low power consumption while retaining the content of SRAM and registers. The kernel LDO can be configured in either main or low power mode. All high-frequency clocks in the kernel power domain are stopped, and the PLL, the RCH and the OSCH crystal oscillators are disabled. The analog modules in the kernel power domain can be turned off/on by software, depending on the state of the kernel LDO.

The device can be woken up from Stop mode by any of the EXTI line, which can be one of the 16 external lines, the LVD output, the WT alarm or the output of analog comparators.

- **ULP Stop** mode

The ULP Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. The kernel LDO is switched off, and the kernel power domain is supplied by the backup LDO. All high-frequency clocks in the kernel power domain are stopped, and the PLL, the RCH and the OSCH crystal oscillators are disabled. All analog modules in the kernel power domain are turned off.

In ULP Stop mode, the LDO output can be configured in four levels from 1.5V to 1.0V. When it is under 1.2V, the static power consumption can be further reduced.

The device can be woken up from ULP Stop mode by any of the EXTI line, which can be one of the 16 external lines, the LVD output, the WT alarm or the output of analog comparators.

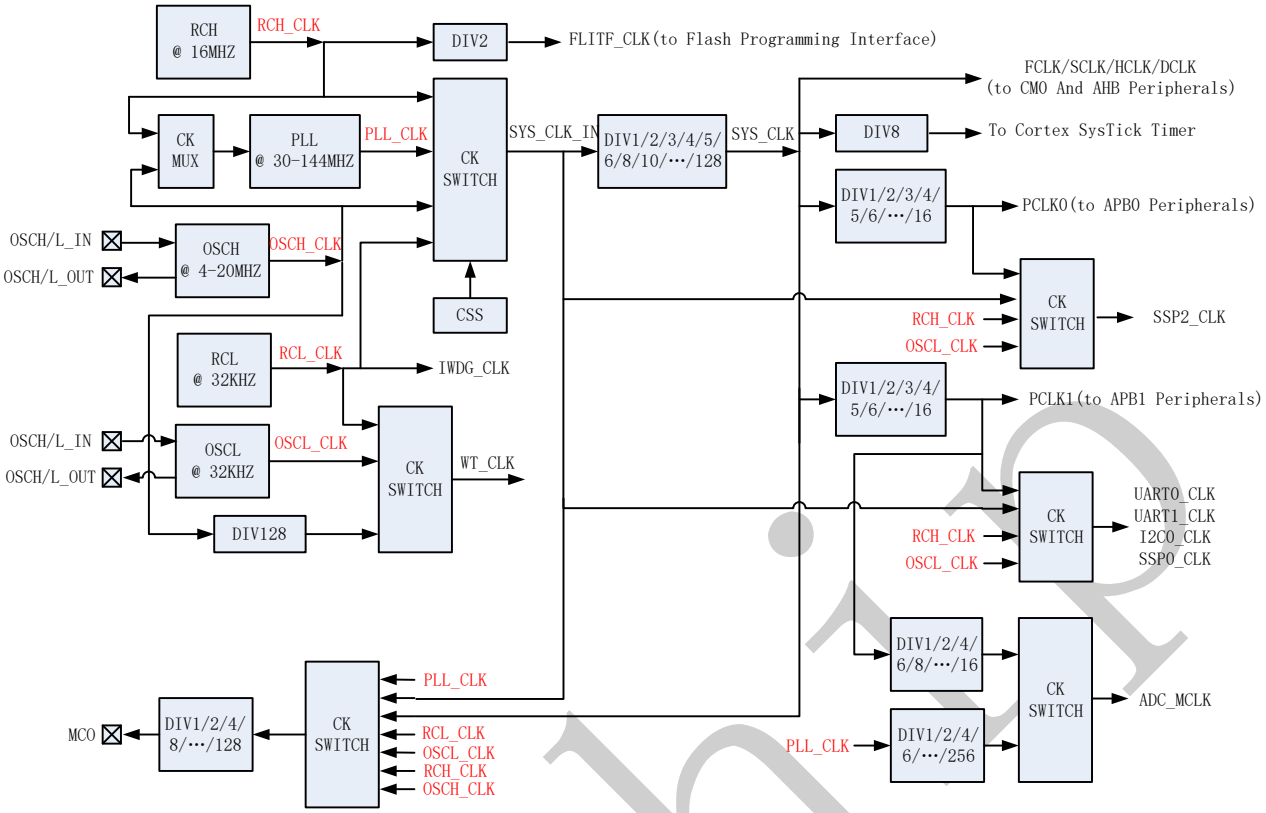
Note: The WT, the IWDG, and the corresponding clock sources are not stopped when entering Stop or ULP Stop mode.

1.7 Clock and startup

System clock selection is performed on startup, and the internal RC 16 MHz oscillator is selected as default CPU clock on reset. An external 4-20 MHz clock or the PLL clock can be selected, in which case they are monitored for failure. If failure is detected, the according clock is isolated and the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled.

OSCH and OSCL reuse the same I/O pins (PF0 and PF1) so that they cannot be used at the same time. These clocks and several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB1) and low-speed APB (APB0) domains. The maximum allowed frequency of the AHB and APB domains is 96 MHz. See Figure 2 for details on the clock tree.

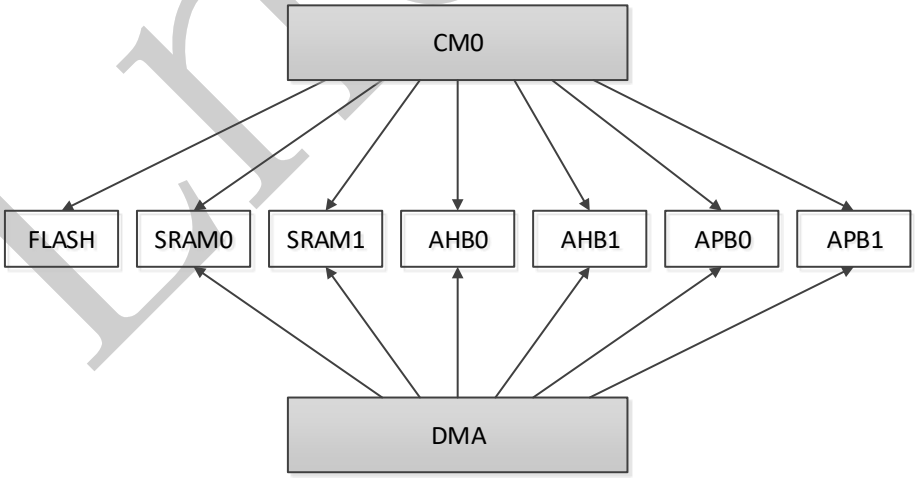
Figure 2. LCM32F037 clock tree



1.8 Multi AHB bus matrix

The 32-bit multi AHB bus matrix interconnects all masters (CPU, DMA) and slaves (Flash, SRAM, AHB, APB peripherals). It manages the access arbitration between the masters.

Figure 3. LCM32F037 bus matrix



1.9 Peripheral interconnection matrix

Several LCM32F037 peripherals have internal interconnections. It allows autonomous communication and efficient synchronization between peripherals. In addition, it discards the software latency and minimizes GPIOs configuration.

Table 1. LCM32F037 peripheral interconnection matrix

Source	Destination	Action
TIMx	TIMx	Timer synchronization or chaining
	ADC	A/D conversion trigger
	DACx	D/A conversion trigger
	ACMPx	Comparator output blanking control
	DMA	Memory transfer trigger
ADC	TIMx	Simulate the watchdog trigger for timers
GPIO WTCLK OSCH/128 MCO	TIM14	Each clock source is connected to the timer's input channel for clock calibration
ACMPx	TIMx	Timer output control, input capture, input trigger
	ADC	A/D conversion trigger
CSS CPU (Hard Fault) LVD ACMPx GPIO	TIM1 TIM15 TIM16 TIM17	Trigger for the internal break events of some timers
GPIO	TIMx	External trigger, or break events
	ADC	A/D conversion trigger
	DACx	D/A conversion trigger
DACx	ACMPx	Comparator input

1.10 General-purpose I/Os (GPIOs)

LCM32F037 contains up to 30 fast I/O pins and can tolerate 5V voltage. Drive capability and slope are configurable in two levels. All GPIOs are high-current capable, with speed selection to better manage internal noise, power consumption and electromagnetic radiation.

Each of the GPIO pins can be configured by software as output (push-pull, open-drain or open-source), as input (floating, pull-up or pull-down) or as peripheral alternate function.

Most of the GPIO pins are shared with digital or analog alternate functions. They contain one or two analog channels, which can be enabled or disabled by software. When the two analog channels are enabled, they can work with each other internally.

The I/Os support remapping of peripheral function. It makes the selection of pins more flexible. Users could make use of peripheral function as many as possible on LCM32F037.

The I/Os configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

1.11 Direct memory access controller (DMA)

The flexible 4-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the following peripherals: SSP, I2C, UART, ADC, DAC, and timers.

1.12 Interrupts and events

1.12.1 Nested vectored interrupt controller (NVIC)

LCM32F037 embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of CPU) and 4 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

1.12.2 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to detect external I/O ports/LVD output/WT alarm/comparator output, generate interrupt/event requests, and wake up the system.

Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal APB1 clock period. Up to 30 GPIOs can be connected to the 16 external interrupt lines.

1.13 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded into LCM32F037. It shares 16 external channels (three OPA outputs, internal Bandgap voltage reference) and 2 internal channels (temperature sensor and VDDA), performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs. The conversion rate is up to 1.5 MSPS. ADC Block diagram is shown in Figure 4.

The ADC supports the use of internal or external reference voltages (2.5V, 3.3V, 4V, 5V, VDDA or external IO).

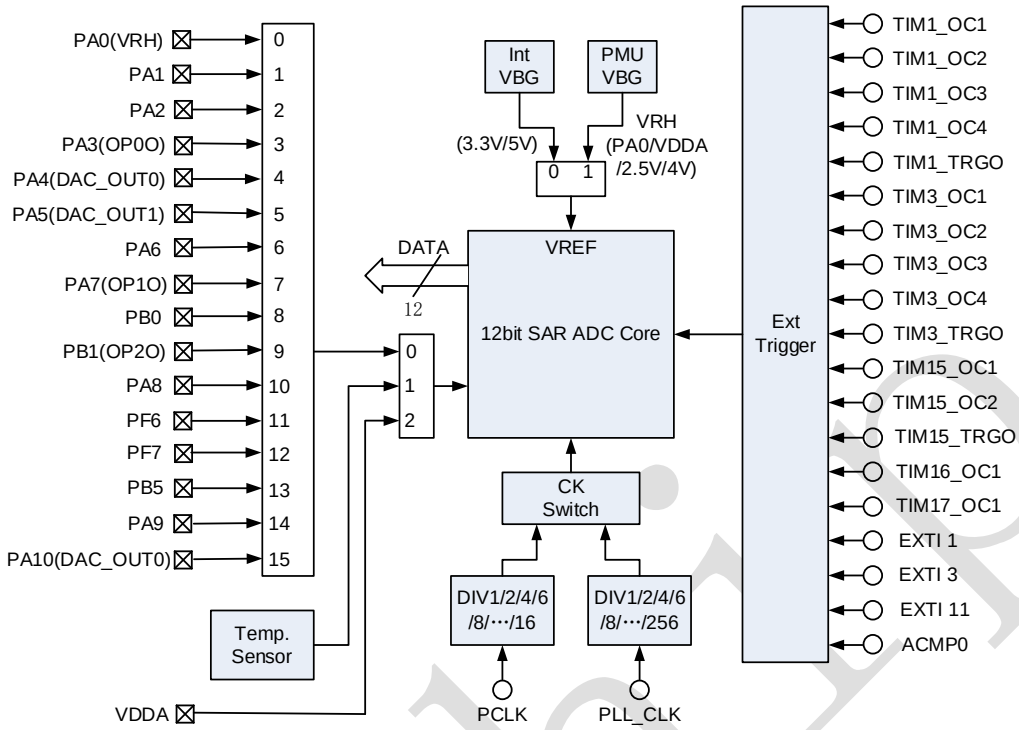
The ADC has an embedded temperature sensor. It can produce a voltage which changes linearly with temperature. It is internally connected to the input channel of ADCIN16.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the timers (TIMx), analog comparators (ACMPs), and external IO can be internally connected to the ADC start trigger. The ADC trigger interconnection diagram is shown in Figure 5. The outputs of DAC and ACMPs can also be used as ADC input through GPIO ports.

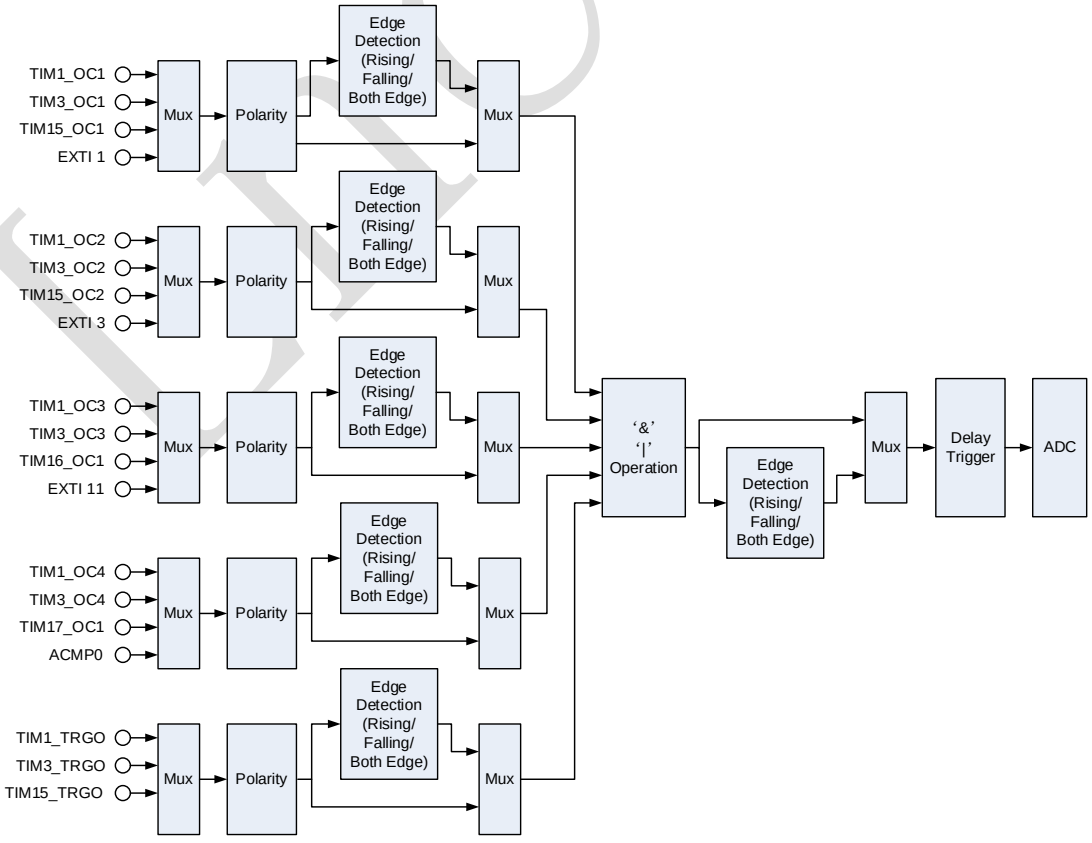
The ADC supports synchronous prescaler of the APB clock (PCLK1), or asynchronous prescaler of the PLL clock. Different clocks make a balance between trigger delay and high-speed work frequency. It also has an embedded 16-depth FIFO with DMA capability.

Figure 4. ADC Block diagram



Note: VRH/OP0O/OP1O/OP2O/DAC0_OUT/DAC1_OUT/OP0OEX/OP1OEX/OP2OEX. These outputs can be transferred to ADC input channels by I/O analog channel loops. The I/O must be configured in analog mode, and both analog channels should be enabled with high impedance externally.

Figure 5. ADC trigger interconnection diagram



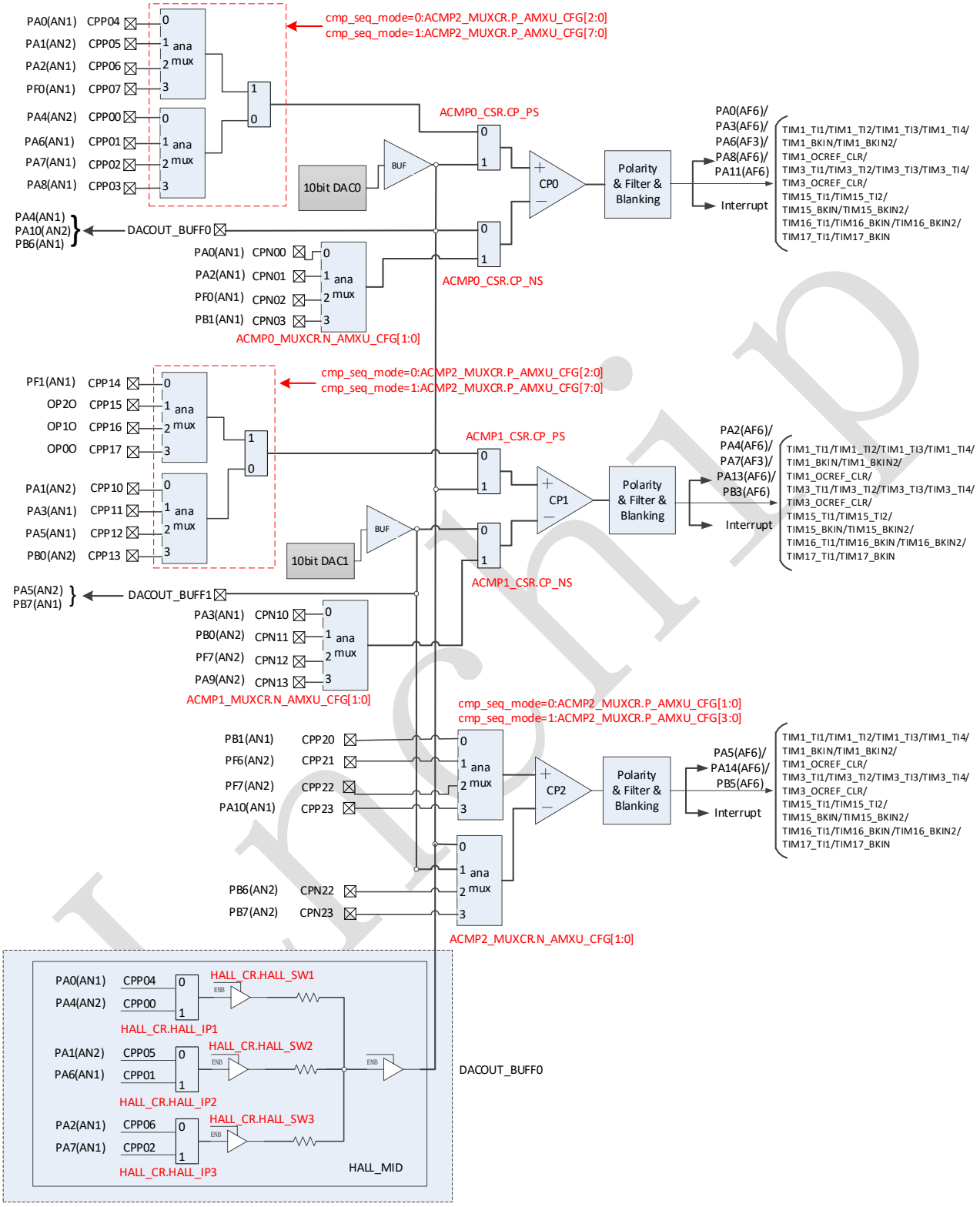
1.14 Digital-to-analog converter (DAC), Analog comparator (ACMP) and HALL_MID

Two 10-bit digital-to-analog converters are embedded into LCM32F037. Each DAC can be used to convert digital signals into analog voltage outputs to I/O ports or three ACMP inputs. The reference voltage of DAC is available among 2.5V, 4V or VDDA independently. Each DAC supports hardware trigger and DMA transfer. Each DAC is able to produce configurable pseudo-random noise waveforms and triangular waveforms by hardware.

Three fast rail-to-rail analog comparators (ACMPs) are embedded into LCM32F037. The ACMP inputs come from internal DAC outputs, HALL_MID outputs or external I/O ports. The external trigger, hysteresis, speed, filtering and polarity of ACMPs are all configurable. Interrupts generated by AMCPs can wake up the system from low power modes. All ACMPs can play the role of triggers for the internal break events of some timers. Two ACMPs can be combined as a window comparator.

One anti-electric force sampling controller (HALL_MID) is embedded into LCM32F037. It can work with DAC and ACMPs, and more details of the interconnection are shown in Figure 6.

Figure 6. DAC, HALL_MID and ACMP interconnection diagram



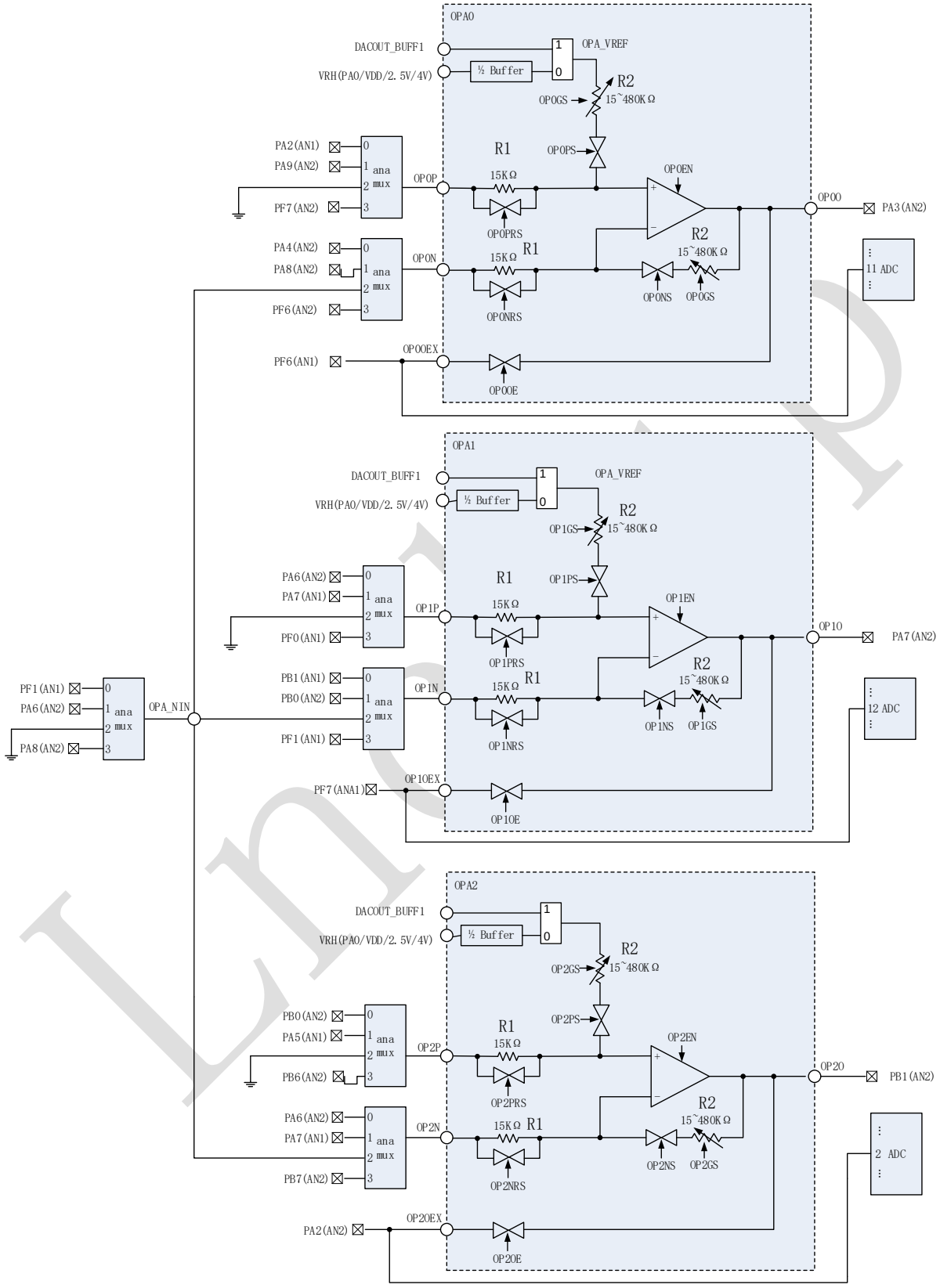
1.15 Operational amplifier (OPA)

There are three embedded OPAs in LCM32F037. The magnification of each OPA is 1/2/4/6/10/16/20/32. The output bias is 1/2 or DAC1_OUT. The three OPAs have following features:

- Input common-mode input voltage: 0V to VDDA
- Input offset voltage: -/+ 5mV (before calibration); -/+ 1mV (after calibration)
- The conversion rate: 5V/us
- Power supply rejection ratio: -60DB (min), -80DB (typ)
- Gain error: +/- 1%
- Temperature drift: 0.1%
- CMRR: 90dB
- The temperature characteristics: the higher the temperature, the larger the magnification. The magnification curve is strictly prohibited to bend down

The OPAs and their interconnection are shown in Figure 7 below.

Figure 7. OPAs and their interconnection



Note: OP0O/OP1O/OP2O outputs can be transferred to ADC input channels by I/O analog channel loops. The I/O must be configured in analog mode, and both analog channels should be enabled with high impedance externally.

1.16 Timers and watchdogs

The LCM32F037 includes an advanced-control timer, five general-purpose timers, a basic timer, two watchdog timers and a SysTick timer. In debug mode, all timer counters can be frozen.

Table 2 compares the features of the advanced-control, general-purpose and basic timers.

Table 2. Timer feature comparison

Timer Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA request Generation	Capture/Compare Channels	Complementary Outputs
Advanced Control	TIM1	16-bit	Up, Down, Up/down	1 to 65536	Yes	4	3
General Purpose	TIM3	16-bit	Up, Down, Up/down	1 to 65536	Yes	4	0
	TIM14	16-bit	Up	1 to 65536	No	1	0
	TIM15	16-bit	Up, Down, Up/down	1 to 65536	Yes	2	2
	TIM16	16-bit	Up, Down, Up/down	1 to 65536	Yes	1	1
	TIM17	16-bit	Up, Down, Up/down	1 to 65536	Yes	1	1
Basic	TIM6	16-bit	Up	1 to 65536	Yes	0	0

1.16.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead-times. It can also be seen as a complete general-purpose timer. The four independent channels can be used separately:

- Input capture
- Output compare
- PWM generation (edge- or center- aligned modes)
- One-pulse mode output

If configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

TIM1 supports delay trigger and error-proof triggering mechanisms. In debug mode, the counter can be frozen.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the timer link feature for synchronization or event chaining.

1.16.2 General-purpose timers (TIM3/14/15/16/17)

The LCM32F037 has five synchronizable general-purpose timers, and the detailed differences are shown in Table 2 above.

TIM3

TIM3 is a synchronizable 4-channel general-purpose timer based on a 16-bit autoreload up/down counter and a 16-bit prescaler.

Tim3 has four independent channels for input capture, output compare, PWM generation, or one-pulse mode output.

TIM3 can work with the advanced-control timer TIM1 through the timer link feature for synchronization or event chaining.

TIM3 generates independent DMA requests.

Tim3 can handle quadrature (incremental) encoder input, as well as the outputs of HALL_MID.

In debug mode, the counter can be frozen.

TIM14

TIM14 is based on a 16-bit autoreload upcounter and a 16-bit prescaler.

Tim14 has an independent channel for input capture, output compare, PWM generation, or one-pulse mode output.

In debug mode, the counter can be frozen.

TIM15/16/17

Tim15/16/17 is based on a 16-bit autoreload up/down counter and a 16-bit prescaler.

TIM15 has two independent channels, and TIM16/17 has an independent channel for input capture, output compare, PWM generation, or one-pulse mode output.

TIM15 has two complementary outputs, and TIM16/17 has a complementary output with programmable inserted dead-times.

TIM15/16/17 generates independent DMA requests.

TIM15/16/17 supports delay trigger and error-proof triggering mechanisms. In debug mode, the counter for TIM15/16/17 can be frozen.

1.16.3 Basic timer (TIM6)

TIM6 can be used as a common 16-bit time base.

TIM6 generates independent DMA requests.

1.16.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It contains a user-defined refreshed window. It is clocked from an independent 32 kHz internal RC and as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

1.16.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB0 clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

1.16.6 System timer (SysTick)

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

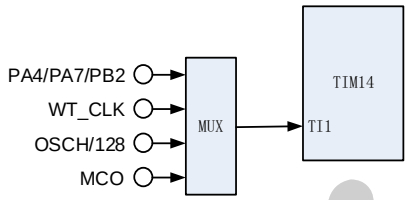
- A 24-bit downcounter

- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

1.16.7 Clock measurement and calibration

The on-line measurement and calibration of each clock source can be made via the input channel TI1 of TIM4.

Figure 8. Clock measurement and calibration



1.16.8 Interconnections between timers

Timers can work together via the timer link feature for synchronization or event chaining. It is shown in the following Table 3.

Table 3. Interconnections between timers

Slave TIM	ITR0	ITR1	ITR2	ITR3
TIM1	TIM15_TRGO	TIM16_OC1	TIM3_TRGO	TIM17_OC1
TIM3	TIM1_TRGO	TIM17_OC1	TIM15_TRGO	TIM14_OC1
TIM15	TIM1_TRGO	TIM3_TRGO	TIM16_OC1	TIM17_OC1

1.17 Watch timer (WT)

The WT belongs to the backup power domain. It is powered by the backup LDO only in ULP Stop mode; while powered by the kernel LDO in other power modes. The WT cannot be reset by system reset sources.

The WT is always used for alarm interrupt, as well as buzzer output. It has following features:

- Programmable clock source:
  - External crystal oscillator (OSCL) at 32.768 kHz
  - Internal low-power RC oscillator (RCL) of 32 kHz
  - External high-speed crystal oscillator (OSCH) divided by 128
- Four clock sources for internal 8-bit timer: 4kHz, 64Hz, 1Hz, 1/60Hz
- 8-bit timer overflow interrupt
- 0.5s period interrupt
- Eight BUZ signal frequencies: four high-speed (8192Hz, 4096Hz, 2048Hz, 1024Hz) and four low-speed (2Hz, 1Hz, 0.5Hz, 0.25Hz). Also supporting reverse signal nBUZ output.

1.18 Inter-integrated circuit (I2C)

The LCM32F037 has an I2C interface, which includes the following features:

- Multimaster and slave modes
- Supporting standard speed (up to 100 kbps) and fast speed (400 kbps to 1 Mbps)
- 7/10-bit addressing

- Independent clock up to 96 MHz
- 8-byte Rx/Tx FIFOs with DMA capability

1.19 Universal asynchronous receiver transmitter (UART)

The LCM32F037 has two UART interfaces, which include the following features:

- Accurate baud rate generation up to 4 Mbps
- 8-byte Rx/Tx FIFOs with DMA capability
- Hardware management of the CTS and RTS signals
- Independent clock up to 96 MHz

1.20 Synchronous Serial Port (SSP)

The LCM32F037 has two SSP interfaces, which include the following features:

- Master and slave modes
- Supporting Motorola SPI, TI SSI and National Semiconductor Microwire protocols
- Programmable 4 to 16-bit frame size
- Independent clock up to 96 MHz
- Able to communicate up to 32 Mbps in master mode and up to 5 Mbps in slave mode
- 8x16 bit Rx/Tx FIFOs with DMA capability

1.21 Cycle Redundancy Check (CRC)

The CRC calculation unit is used to get a CRC code from an 8/16/32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

1.22 Divider (DIV)

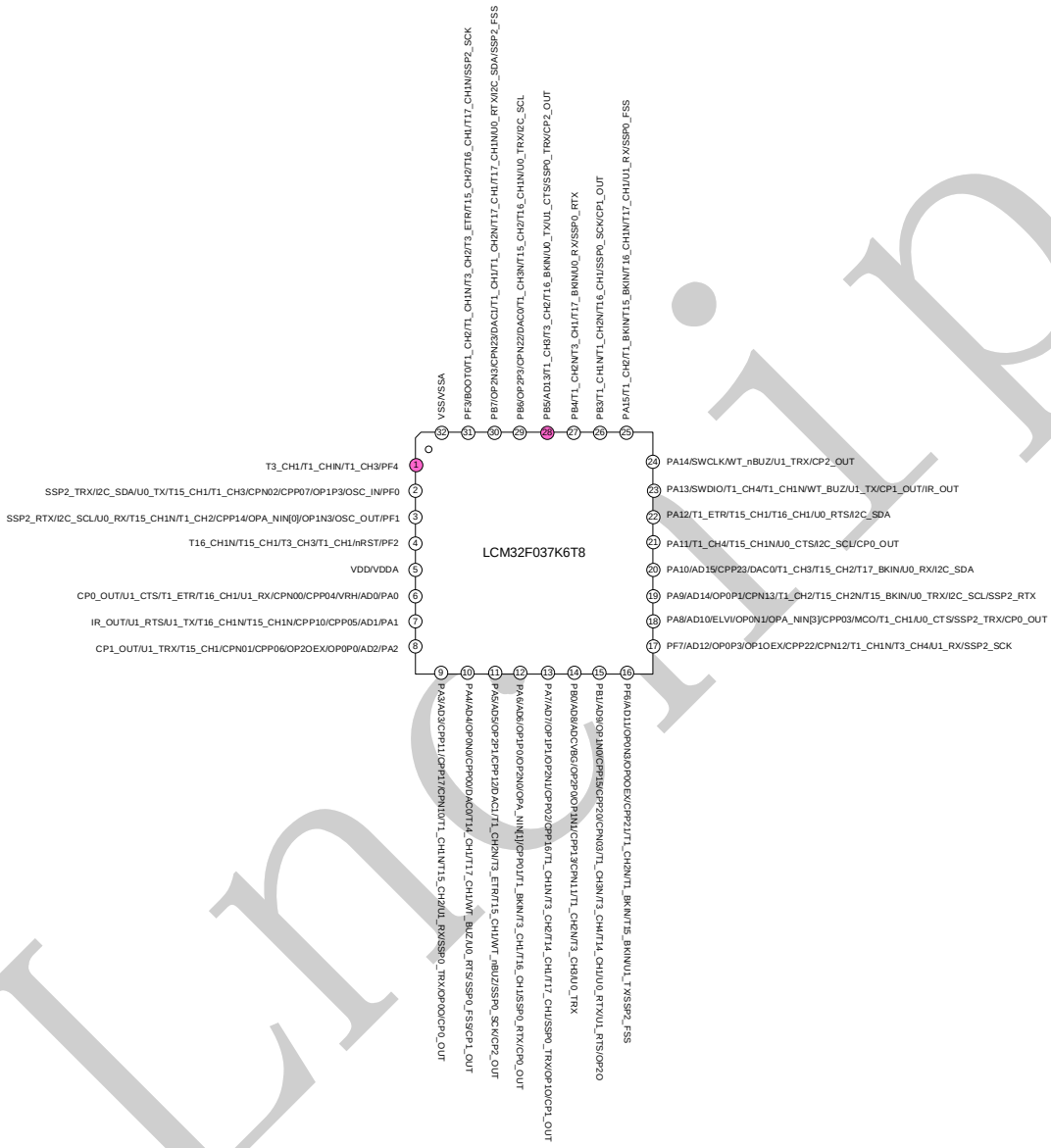
The DIV supports 64/32 or 32/32 signed divisions within 32 cycles.

1.23 Serial wire debug port (SW-DP)

An embedded ARM SW-DP interface enables either a serial wire debug probe to be connected to the target. Only two I/Os (SWDIO and SWCLK) are used for debug by GPIO alternate function.

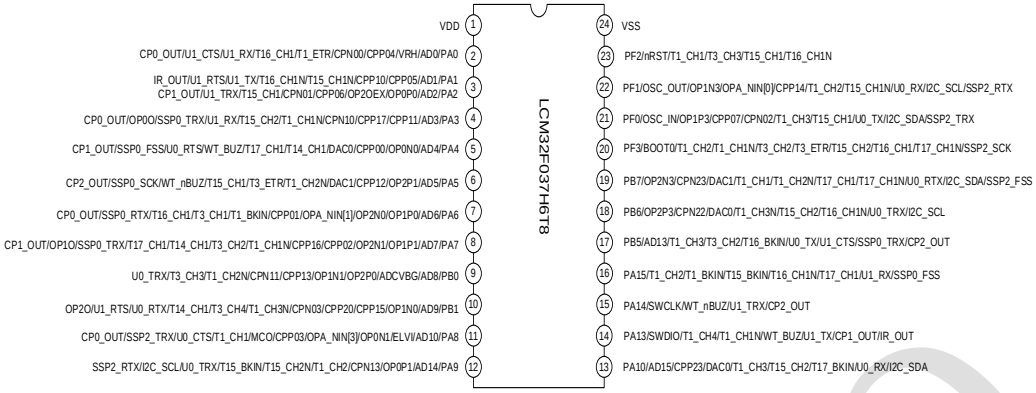
2. Pinouts and pin description

Figure 9. LCM32F037K6T8 LQFP32 pinout



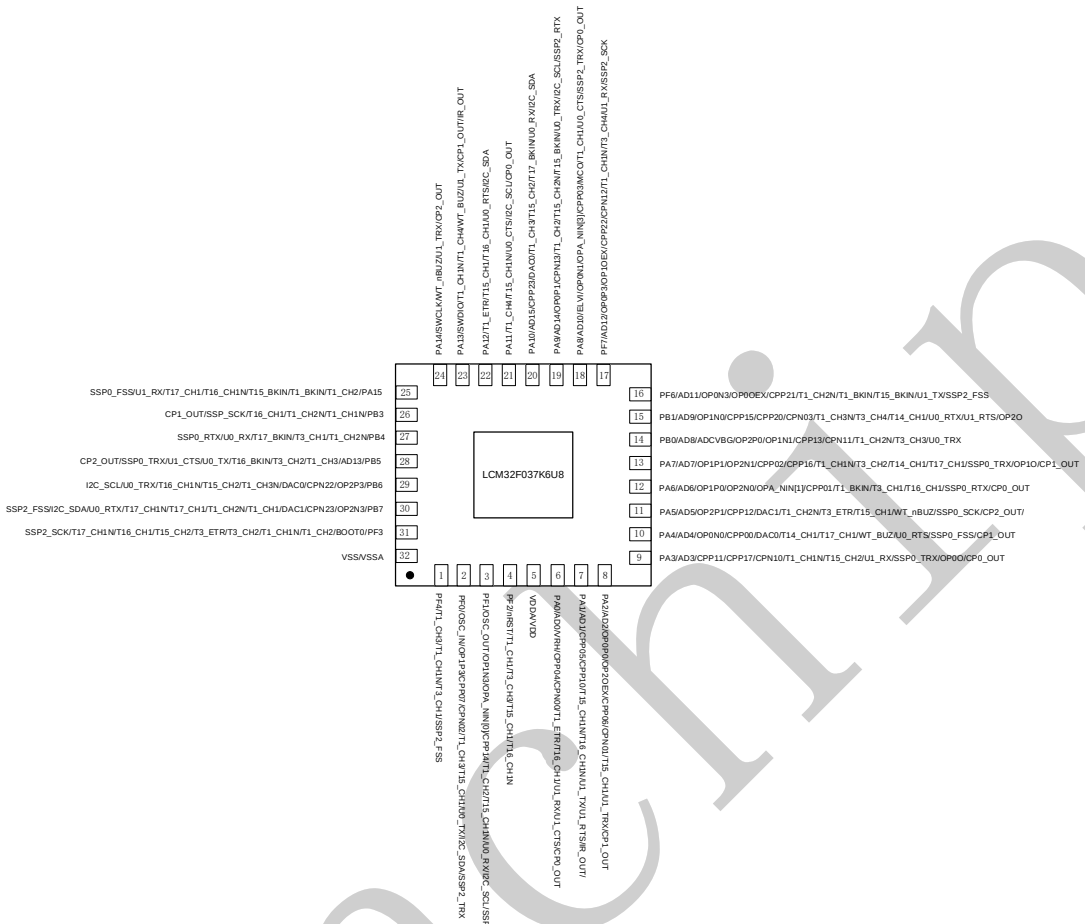
(See Table 5 for detailed pin definitions)

Figure 10. LCM32F037H6S8 SSOP24 pinout



(See Table 5 for detailed pin definitions)

Figure 11. LCM32F037K6U8 QFN32 pinout



(See Table 5 for detailed pin definitions)

Table 4. Abbreviations used for pin definitions

Name		Abbreviation	Definition
Pin name		The pin function and name stay the same during/after reset unless specifically stated in brackets	
Pin type		S	Power pin
		I	Only input pin
		I/O	Input/output pin
I/O structure		1ANA	Only one analog alternate channel
		2ANA	Two analog alternate channels and two normal analog switches (PAD to analog switches with ESD resistance)
		2OP	Two analog alternate channels and two analog switches of low inner resistance (PAD directly to analog switch for OPA)
		ANA_OP	Two analog alternate channels, one normal analog switch and one analog switch of low inner resistance
Note		All I/Os are floating input during/after reset, unless specified in *Note*	
Pin Function	Optional alternate function	Features configured by GPIOx_AFL/H, GPIOx_MODE registers (digital alternate)	
	External alternate function	Features configured by the SYSCTRL register which has higher priority than optional alternate function (digital alternate)	
	Analog alternate function 1	Analog function 1 configured by SYSCTRL or GPIOx_AFL/H, GPIOx_MODE register	
	Analog alternate function 2	Analog function 2 configured by SYSCTRL or GPIOx_AFL/H, GPIOx_MODE register	

Table 5. LCM32F037 pin definitions

Pin number		Pin name (after reset)	Pin type	I/O structure	Optional alternate function	External function	Analog alternate function (AN)	
LQFP32/ QFN32	SSOP24						AN1	AN2
		TESTEN				Test		
1		PF4	I/O	1ANA	SSP2_FSS/TIM1_CH1N/ TIM1_CH3/TIM3_CH1/			
2	21	PF0	I/O	2OP	SSP2_TXD/ I2C0_SDA/ TIM1_CH3/ TIM15_CH1/ UART0_TX/ SSP2_RXD		CPN02[1]/ OP1P3/ CPP07	OSCL_IN / OSCH_IN
3	22	PF1	I/O	2OP	SSP2_RXD/ I2C0_SCL/ TIM1_CH2/ TIM15_CH1N/ URAT0_RX/ SSP2_TXD		CPP14 / OP1N3/ OPA_NIN2	OSCL_OUT / OSCH_OUT
4	23	PF2(nRST)	I/O	1ANA	TIM1_CH1/ TIM3_CH3/ TIM15_CH1/TIM16_CH1N	nRST[2]		
	24	VSS/VSSA	S					
5	1	VDDA	S					
5	1	VDDH	S					
6	2	PA0	I/O	2ANA	UART1_CTS/ TIM1_ETR/ TIM16_CH1/ UART1_RX/ CP0_OUT		ADCIN[0] / CPP04 / CPN00	VRH
7	3	PA1	I/O	2ANA	EVENTOUT/ UART1_RTS/ TIM16_CH1N/ UART1_TX/ TIM15_CH1N/ IR_OUT		ADCIN[1]	CPP05/ CPP10
8		PA2	I/O	2OP	TIM15_CH1/ UART1_TX/ CP1_OUT/ UART1_RX		CPN01/ OP0P0/ CPP06	OP2OEX / ADCIN[2]
9	4	PA3	I/O	ANA_OP	TIM15_CH2/ UART1_RX/ TIM1_CH1N/ SSP0_TXD/ CP0_OUT/ SSP0_RXD		ADCIN[3] / CPN10/ CPP11	OP0O/ CPP17
10	5	PA4	I/O	2OP	SSP0_FSS/UART0_RTS/ TIM17_CH1/ TIM14_CH1/ WT_BUZ/ CP1_OUT		DAC_OUT0	ADCIN[4] / OP0N0 / CPP00
11	6	PA5	I/O	2OP	SSP0_SCK/ TIM15_CH1/ TIM1_CH2N/WT_nBuz/ CP2_OUT/ TIM3_ETR		ADCIN[5] / OP2P1 / CPP12	DAC_OUT1
12	7	PA6	I/O	ANA_OP	SSP0_RXD/TIM3_CH1/ TIM1_BKIN/CP0_OUT/ TIM16_CH1/ EVENTOUT/ SSP0_TXD		ADCIN[6] / CPP01	OP1P0 / OP2N0/ OPA_NIN3
13	8	PA7	I/O	2OP	SSP0_TXD/ TIM3_CH2/ TIM1_CH1N/CP1_OUT/ TIM14_CH1/ TIM17_CH1/ EVENTOUT/ SSP0_RXD		ADCIN[7] / OP1P1/ OP2N1/ CPP02	OP1O/ CPP16
14	9	PB0	I/O	ANA_OP	EVENTOUT/ TIM3_CH3/ TIM1_CH2N/ UART0_TX/ UART0_RX		ADCVBG	ADCIN[8]/ CPP13/ OP2P0/ CPN11/ OP1N1
15	10	PB1	I/O	2OP	TIM14_CH1/TIM3_CH4/ TIM1_CH3N/UART1_RTS/ UART0_RX/UART0_TX		ADCIN[9]/ CPP20/ OP1N0/ CPN03	OP2O/ CPP15
16		PF6	I/O	ANA_OP	SSP2_FSS/TIM1_CH2N/ TIM1_BKIN/UART1_TX/ TIM15_BKIN/EVENTOUT		ADCIN[11]/ OP0OEX	OP0N3/ CPP21
17		PF7	I/O	ANA_OP	SSP2_SCK/TIM1_CH1N/ TIM3_CH4/ URAT1_RX		ADCIN[12]/ OP1OEX	OP0P3 / CPN12/ CPP22
18	11	PA8	I/O	ANA_OP	MCO/UART0_CTS/ TIM1_CH1/ EVENTOUT/ SSP2_TXD/ SSP2_RXD/ CP0_OUT		ADCIN[10]/ ELVI / CPP03	OP0N1/ OPA_NIN1
19	12	PA9	I/O	ANA_OP	TIM15_CH2N/ TIM15_BKIN/ UART0_TX/ TIM1_CH2/ I2C0_SCL/ SSP2_RXD/		ADCIN[14]	CPN13/ OP0P1

					SSP2_TXD/ UART0_RX			
20	13	PA10	I/O	2ANA	TIM15_CH2/ TIM17_BKIN/ UART0_RX/ TIM1_CH3/ I2C0_SDA		ADCIN[15]/ CPP23	DAC_OUT0
21		PA11	I/O	2ANA	EVENTOUT/ UART0_CTS/ TIM1_CH4/ TIM15_CH1N/ CP0_OUT/ I2C0_SCL			
22		PA12	I/O	1ANA	EVENTOUT/ UART0_RTS/ TIM1_ETR/ TIM16_CH1/ TIM15_CH1/ I2C0_SDA/			
23	14	PA13	I/O	1ANA	IR_OUT/ TIM1_CH1N/ TIM1_CH4/ UART1_TX/ WT_BUZ/ CP1_OUT	SWDIO[3]		
24	15	PA14	I/O	1ANA	UART1_TX/ WT_nBUZ/ CP2_OUT/ UART1_RX	SWCLK[3]		
25	16	PA15	I/O	1ANA	SSP0_FSS/UART1_RX/ TIM17_CH1/EVENTOUT/ TIM1_CH2/TIM16_CH1N/ TIM1_BKIN/TIM15_BKIN			
26		PB3	I/O	1ANA	SSP0_SCK/TIM1_CH1N/ TIM1_CH2N/TIM16_CH1/ CP1_OUT			
27		PB4	I/O	1ANA	SSP0_RXD/TIM3_CH1/ TIM1_CH2N/UART0_RX/ TIM17_BKIN/SSP0_TXD			
28	17	PB5	I/O	1ANA	SSP0_TXD/TIM3_CH2/ TIM16_BKIN/TIM1_CH3/ UART0_TX/UART1_CTS/ CP2_OUT/ SSP0_RXD		ADCIN[13]	
29	18	PB6	I/O	ANA_OP	UART0_TX/I2C0_SCL/ TIM16_CH1N/TIM15_CH2/ TIM1_CH3N/ UART0_RX		DAC_OUT0	OP2P3 / CPN22
30	19	PB7	I/O	ANA_OP	UART0_RX/I2C0_SDA/ TIM17_CH1N/TIM1_CH2N/ UART0_TX/TIM1_CH1/ TIM17_CH1/SSP2_FSS		DAC_OUT1	OP2N3/ CPN23
31	20	PF3(BOOT0)	I/O	1ANA	SSP2_SCK/ TIM1_CH1N/ TIM1_CH2/ TIM3_CH2/ TIM15_CH2/ TIM16_CH1/ TIM17_CH1N/ TIM3_ETR	BOOT0[4]		
32		VSS/VSSA	S					

Note: 1. ACMP and OPA input pin formats:

ACMP: ACMP number + Pin polarity + Input port; OPA: OPA number + Pin polarity + Input port

Example: CPP11 means ACMP1, positive input, port1

OP2N3 means OPA2, negative input, port3

2. After power-up reset, this pin is configured to the external reset pin nRST by default

3. After system reset, these pins are configured as optional alternate functions SWDIO (internal pull-up) and SWCLK (internal pull-down)

4. Depending on the option byte configuration, the BOOT0 pin can be used to select one of three boot options during system reset

5. The I/O drive strength 4mA/8mA when powered by 3.3V, and 8mA/16mA when powered by 5V

Table 6. GPIOA optional alternate function mapping

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	UART1_CTS	TIM1_ETR	TIM16_CH1	UART1_RX	-	CP0_OUT	-
PA1	EVENTOUT	UART1_RTS	TIM16_CH1N	-	UART1_TX	TIM15_CH1N		IR_OUT-
PA2	TIM15_CH1	UART1_TX	-	-	-		CP1_OUT	UART1_RX
PA3	TIM15_CH2	UART1_RX	-	-	TIM1_CH1N	SSP0_TXD	CP0_OUT	SSP0_RXD
PA4	SSP0_FSS	UART0_RTS	-	TIM17_CH1	TIM14_CH1	WT_BUZ	CP1_OUT	-
PA5	SSP0_SCK	-	-	TIM15_CH1	TIM1_CH2N	WT_nBuz	CP2_OUT	TIM3_ETR-
PA6	SSP0_RXD	TIM3_CH1	TIM1_BKIN	CP0_OUT	-	TIM16_CH1	EVENTOUT	SSP0_TXD
PA7	SSP0_TXD	TIM3_CH2	TIM1_CH1N	CP1_OUT	TIM14_CH1	TIM17_CH1	EVENTOUT	SSP0_RXD
PA8	MCO	UART0_CTS	TIM1_CH1	EVENTOUT	SSP2_TXD	SSP2_RXD	CP0_OUT	
PA9	TIM15_CH2N	TIM15_BKIN	UART0_TX	TIM1_CH2	I2C0_SCL	SSP2_RXD	SSP2_TXD	UART0_RX
PA10	TIM15_CH2	TIM17_BKIN	UART0_RX	TIM1_CH3	I2C0_SDA	-		
PA11	EVENTOUT	UART0_CTS	TIM1_CH4	TIM15_CH1N	-		CP0_OUT	I2C0_SCL
PA12	EVENTOUT	UART0_RTS	TIM1_ETR	TIM16_CH1	TIM15_CH1			I2C0_SDA
PA13	SWDIO	IR_OUT	TIM1_CH1N	TIM1_CH4	UART1_TX	WT_Buz	CP1_OUT	-
PA14	SWCLK	UART1_TX	-	-	-	wt_nBuz	CP2_OUT	UART1_RX
PA15	SSP0_FSS	UART1_RX	TIM17_CH1	EVENTOUT	TIM1_CH2	TIM16_CH1N	TIM1_BKIN	TIM15_BKIN

Table 7. GPIOB optional alternate function mapping

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	-	UART0_TX	-	UART0_RX	
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	-	UART1_RTS	UART0_RX		UART0_TX
PB3	SSP0_SCK	TIM1_CH1N	TIM1_CH2N	TIM16_CH1			CP1_OUT	-
PB4	SSP0_RXD	TIM3_CH1	TIM1_CH2N	UART0_RX		TIM17_BKIN	-	SSP0_TXD
PB5	SSP0_TXD	TIM3_CH2	TIM16_BKIN	TIM1_CH3	UART0_TX	UART1_CTS	CP2_OUT	SSP0_RXD
PB6	UART0_TX	I2C0_SCL	TIM16_CH1N	TIM15_CH2	TIM1_CH3N	-	-	UART0_RX
PB7	UART0_RX	I2C0_SDA	TIM17_CH1N	TIM1_CH2N	UART0_TX	TIM1_CH1	TIM17_CH1	SSP2_FSS

Table 8. GPIOF optional alternate function mapping

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PF0	SSP2_TXD	I2C0_SDA	TIM1_CH3	TIM15_CH1	UART0_TX	-	-	SSP2_RXD
PF1	SSP2_RXD	I2C0_SCL	TIM1_CH2	TIM15_CH1N	URAT0_RX	-	-	SSP2_TXD
PF2	-	-	TIM1_CH1	TIM3_CH3	TIM15_CH1	TIM16_CH1N	-	-
PF3	SSP2_SCK	TIM1_CH1N	TIM1_CH2	TIM3_CH2	TIM15_CH2	TIM16_CH1	TIM17_CH1N	TIM3_ETR
PF4	SSP2_FSS	TIM1_CH1N	TIM1_CH3	TIM3_CH1	-	-		-
PF6	SSP2_FSS	TIM1_CH2N	TIM1_BKIN	-	UART1_TX	TIM15_BKIN	EVENTOUT	
PF7	SSP2_SCK	TIM1_CH1N	TIM3_CH4	-	UART1_RX	-	-	

3. Memory mapping

Figure 12. LCM32F037 memory mapping

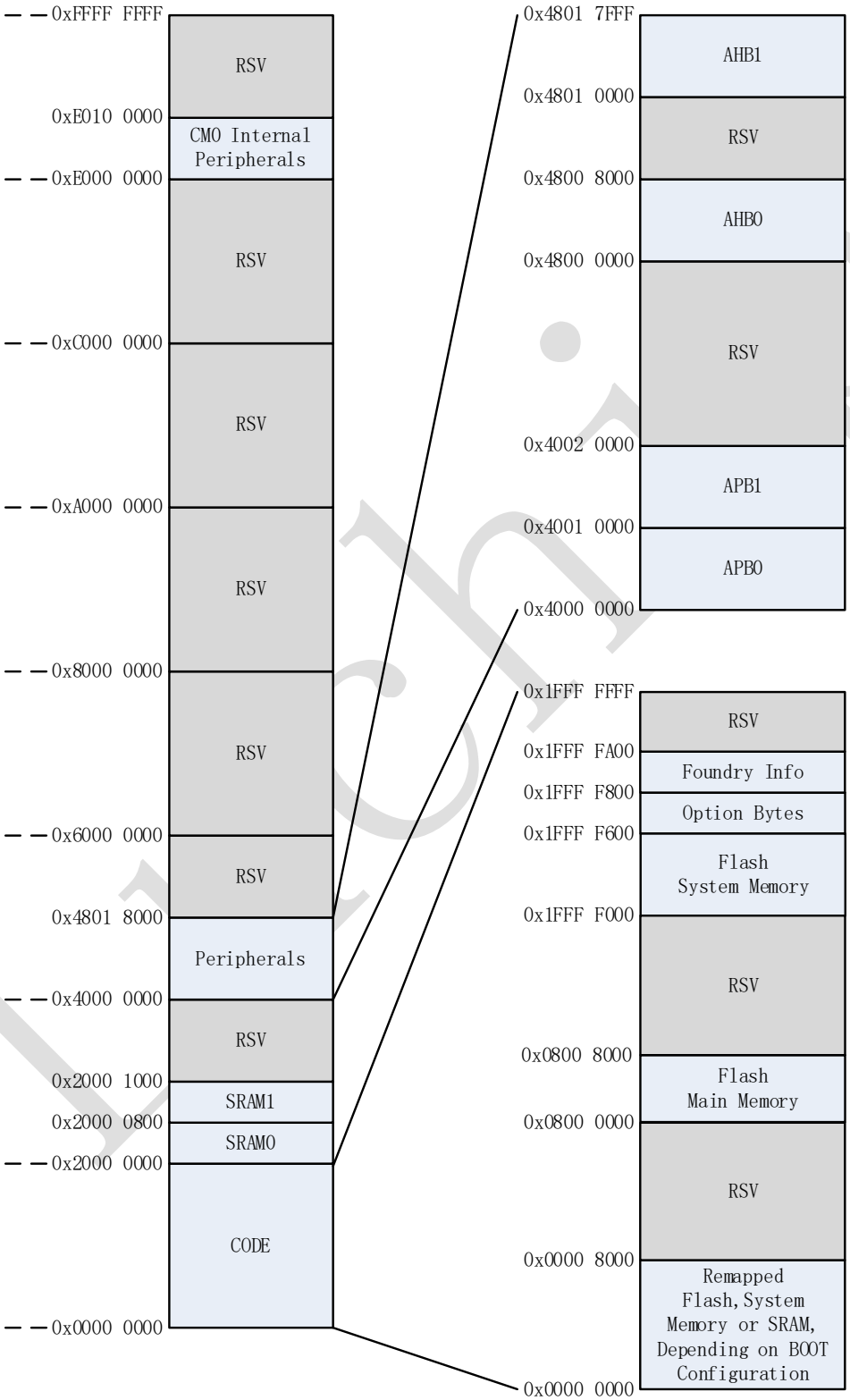


Table 9. LCM32F037 register boundary addresses

Bus	Address range	Size	Peripheral
APB0	0x4000 0000 - 0x4000 0FFF	4KB	RSV
	0x4000 1000 - 0x4000 1FFF	4KB	
	0x4000 2000 - 0x4000 2FFF	4KB	
	0x4000 3000 - 0x4000 3FFF	4KB	
	0x4000 4000 - 0x4000 4FFF	4KB	
	0x4000 5000 - 0x4000 5FFF	4KB	
	0x4000 6000 - 0x4000 6FFF	4KB	SSP2
	0x4000 7000 - 0x4000 7FFF	4KB	RSV
	0x4000 8000 - 0x4000 8FFF	4KB	
	0x4000 9000 - 0x4000 9FFF	4KB	TIM6
	0x4000 A000 - 0x4000 AFFF	4KB	TIM14
	0x4000 B000 - 0x4000 BFFF	4KB	TIM3
	0x4000 C000 - 0x4000 CFFF	4KB	RSV
	0x4000 D000 - 0x4000 DFFF	4KB	WWDG
	0x4000 E000 - 0x4000 EFFF	4KB	RSV
	0x4000 F000 - 0x4000 FFFF	4KB	
APB1	0x4001 0000 - 0x4001 0FFF	4KB	TIM1
	0x4001 1000 - 0x4001 1FFF	4KB	EXTI
	0x4001 2000 - 0x4001 2FFF	4KB	RSV
	0x4001 3000 - 0x4001 3FFF	4KB	I2C0
	0x4001 4000 - 0x4001 4FFF	4KB	UART0
	0x4001 5000 - 0x4001 5FFF	4KB	UART1
	0x4001 6000 - 0x4001 6FFF	4KB	RSV
	0x4001 7000 - 0x4001 73FF	1KB	CHIPCTRL
	0x4001 7400 - 0x4001 77FF	1KB	IWDG
	0x4001 7800 - 0x4001 7BFF	1KB	WT
	0x4001 7C00 - 0x4001 7FFF	1KB	ANACTRL
	0x4001 8000 - 0x4001 8FFF	4KB	SSP0
	0x4001 9000 - 0x4001 9FFF	4KB	RSV
	0x4001 A000 - 0x4001 AFFF	4KB	ADC
	0x4001 B000 - 0x4001 BFFF	4KB	TIM15
	0x4001 C000 - 0x4001 CFFF	4KB	TIM16
	0x4001 D000 - 0x4001 DFFF	4KB	FLASH CTRL
	0x4001 E000 - 0x4001 EFFF	4KB	TIM17
	0x4001 F000 - 0x4001 FFFF	4KB	RSV
	0x4002 0000 - 0x47FF FFFF	~128MB	RSV
AHB0	0x4800 0000 - 0x4800 01FF	512B	GPIOA
	0x4800 0200 - 0x4800 03FF	512B	GPIOB
	0x4800 0400 - 0x4800 05FF	512B	RSV
	0x4800 0600 - 0x4800 07FF	512B	
	0x4800 0800 - 0x4800 09FF	512B	
	0x4800 0A00 - 0x4800 0BFF	512B	GPIOF
	0x4800 0C00 - 0x4800 0DFF	512B	RSV
	0x4800 0E00 - 0x4800 0FFF	512B	
	0x4800 1000 - 0x4800 1FFF	4KB	
	0x4800 2000 - 0x4800 2FFF	4KB	
	0x4800 3000 - 0x4800 3FFF	4KB	
	0x4800 4000 - 0x4800 4FFF	4KB	DMA
	0x4800 5000 - 0x4800 5FFF	4KB	RSV
	0x4800 6000 - 0x4800 6FFF	4KB	

	0x4800 7000 - 0x4800 7FFF	4KB	SYSCTRL
	0x4800 8000 - 0x4800 FFFF	32KB	RSV
AHB1	0x4801 0000 - 0x4801 0FFF	4KB	RSV
	0x4801 1000 - 0x4801 1FFF	4KB	CRC
	0x4801 2000 - 0x4801 2FFF	4KB	RSV
	0x4801 3000 - 0x4801 3FFF	4KB	
	0x4801 4000 - 0x4801 4FFF	4KB	DIV
	0x4801 5000 - 0x4801 5FFF	4KB	RSV
	0x4801 6000 - 0x4801 6FFF	4KB	
	0x4801 7000 - 0x4801 7FFF	4KB	

4. Electrical characteristics

4.1 Absolute maximum values

Stresses above the absolute maximum values may cause permanent damage to the device. These values are operating conditions, and it is recommended to use the device in the scope of these specifications. Exposure to maximum value conditions for extended periods may affect device reliability.

Table 10. Voltage characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD} /V_{DDA}	-	-0.3	-	5.5V	V
Input voltage	V_{IN}	-	-0.3	-	V_{DD}+0.3	

Note: All voltages are referenced to VSS

Table 11. Current characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Total current into VDD power lines	I_{VDD}	-	-	-	100	mA
Total current out of VSS ground lines	I_{VSS}	-	-	-	100	
Injected current on the pin	I_{INJ}	$V_{IN}>V_{DD}$ or $V_{IN}<V_{SS}$	-4	-	4	
		$V_O>V_{DD}$ or $V_O<V_{SS}$	-4	-	4	
Total injection current	ΣI_{INJ}	-	-20	-	20	

Table 12. Temperature characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Ambient temperature	T_A	-	-40	-	125	℃
Storage temperature	T_{STG}	-	-55	-	125	
Junction temperature	T_J	-	-	-	150	
Thermal resistance	θ_{JA}	LQFP-32	-	78	-	℃/W
		SSOP-24	-	THD	-	
		TSSOP20				
Total power consumption	P_D	-	-	-	400	mW

Table 13. ESD protection and latch-up characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
HBM	V_{HBM}	MIL-STD-883H	±4000	-	-	V
MM	V_{MM}	JESD22-A115	±200	-	-	
CDM	V_{CDM}	JESD22-C101E	±1000	-	-	
Static latch-up	I_{LAT}	JEDEC standard NO.78D 2011.11	±100	-	-	mA
V_{DD} overvoltage	V_{LAT}		6.5	-	-	V

4.2 Recommended operating conditions

Table 14. Operating conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Standard operating voltage	V_{DD}	-40 to 105℃	1.8	-	5.5	V
Analog operating voltage (ADC/DAC)	V_{DDA}	-40 to 105℃	2.4	-	5.5	V
CPU clock frequency	F_{CPU}	V_{DD}＞1.8V	0	-	48	MHz
		V_{DD}＞2.2V	0	-	96	
Power-on reset threshold	V_{POR}	-	-	1.8	-	V
Power-on reset latency	t_{PWRT}	-	1	5	-	ms
VDD rise time rate	S_{VDD}	Make sure that an internal power-on reset signal can be generated	0.1	-	1000	V/ms
RAM holding voltage	V_{DR}	T_A=-40 to 105℃	1.0	-	-	V

4.3 DC electrical characteristics

The typical operating voltage of the device is 3.3V/5.0V. Here the values are tested with VDD=3.3V (T_A = 25℃) unless stated specifically. DC electrical characteristics are still being refined and the TBD section will be updated gradually.

Table 15. Current consumption

Parameter	Symbol	Peripheral states	Conditions	Minimum	Typical (3.3V/5V)	Maximum	Unit
Supply current in Run mode	I_{Run}	Forbidden	MCLK=8MHz, RCH/2	-	0.627/0.73	-	mA
			MCLK=16MHz, RCH	-	0.788/0.881	-	
			MCLK=24MHz, PLL ON	-	1.655/2.167	-	
			MCLK=48MHz, PLL ON	-	1.807/2.277	-	
			MCLK=72MHz, PLL ON	-	3.26/4.32	-	
		Open all, ADC sampling on	MCLK=8MHz, RCH/2	-	5.63/7.23	-	
			MCLK=16MHz, RCH	-	8.87/10.76	12.09	
			MCLK=48MHz, PLL ON	-	21.24/24.1	-	
			MCLK=72MHz, PLL ON	-	27.58/31.76	-	
Supply current in Sleep mode	I_{Sleep}	Off	MCLK=8MHz, RCH/8	-	-	-	mA
			MCLK=16MHz, RCH/4	-	-	-	
			MCLK=24MHz, RCH/2	-	-	-	
			MCLK=48MHz, RCH/1	-	-	-	
Supply current in Stop mode	I_{Stop}	Off	All modules are closed	-	80/100	-	uA

Note: 1. All I/Os are low output without loading; 2. All modules have no load only with clock on unless specifically stated

Table 16. Current consumption in Stop/ULP Stop modes

Mode	Description	Supply voltage	Kernel voltage	Minimum	Typical	Maximum	Unit
Stop mode	Turn off the CPU and peripheral clocks, the kernel LDO is set to low power mode	3.3V	1.5V	-	80	-	uA
		5V		-	100	-	

ULP Stop mode	Turn off all clocks and PLL, the kernel LDO is off, the backup LDO is on with different voltage output	3.3v	1.5V	-	11	-	
		5V		-	18	-	
		3.3v	1.2V	-	4	-	
		5V		-	5	-	
		3.3v	1.0V	-	3	-	
		5V		-	4	-	

4.4 I/O port characteristics

Table 17. I/O characteristics

Parameter	Symbol	Conditions		Minimum	Typical	Maximum	Unit
Input high level voltage	V_{IH}	All I/Os		0.7*V_{DD}	-	V_{DD}	V
Input low level voltage	V_{IL}	All I/Os				0.3 V_{DD}	
Input hysteresis	V_{HYS}	All I/Os			TBD		mV
Output pin sourcing current	I_{OH}	V_{DD}=3.3V, V_{OH}=0.7*V_{DD}	Weak drive (DS=0)	-	12	-	mA
			Strong drive (DS=1)	-	-	-	mA
		V_{DD}=5V, V_{OH}=0.7*V_{DD}	Weak drive (DS=0)	-	27	-	mA
			Strong drive (DS=1)	-	-	-	mA
Output pin sink current	I_{OL}	V_{DD}=3.3V, V_{OL}=0.4V	Weak drive (DS=0)	-	9		mA
			Strong drive (DS=1)	-	18	-	mA
		V_{DD}=5V, V_{OL}=0.6V	Weak drive (DS=0)		20		mA
			Strong drive (DS=1)	-	36	-	mA
Total current	I_{total}	-	All ports	-	TBD	-	mA
Weak pull-up resistor	R_{pu}	V_{IN}=NULL		-	80	-	kΩ
Weak pull-down resistor	R_{pd}	V_{IN}=NULL		-	33	-	kΩ
Input leakage current (high temperature)	I_{IL}	V_{SS}＜V_{PIN}＜V_{DD},T_A=85℃		-	±20	±100	nA
Filter width	T_{PW} (I/O)	External reset pin		-	2	4	us

4.5 System reset and voltage monitoring

Table 18. System reset and monitoring characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Band gap reference	V_{BG}	1.8 to 5.5V, -40 to 105°C	1.24	1.25	1.26	V
Power-on reset threshold	V_{POR}	0V power on to VDD, -40 to 105°C	1.793	1.825	1.869	V
Power down reset threshold	V_{PDR}	VDD power down to 0V, -40 to 105°C	1.695	1.728	1.77	V
LVR level selection	V_{LVR}	LVRS=000	-	1.8	-	V
		LVRS=001	-	1.93	-	V
		LVRS=010	-	2.13	-	
		LVRS =011	-	2.61	-	
		LVRS=100	-	2.94	-	
		LVRS=101	-	3.18	-	
		LVRS=110	-	3.63	-	

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
		LVRS=111	-	-	-	
LVR hysteresis	$V_{HYS(LVR)}$	-	-	100	-	mV
LVR current	I_{LVR}	Sleep mode on	-	20	-	uA
LVD level selection	V_{LVD}	LVLS= 000	-	-	-	V
		LVLS = 001	-	-	-	
		LVLS = 010	-	-	-	
		LVLS = 011	-	-	-	
		LVLS = 100	-	-	-	
		LVLS = 101	-	-	-	
		LVLS = 110	-	-	-	
		LVLS = 111	-	-	-	
LVD hysteresis	$V_{HYS(LVD)}$	-	100	-	200	mV
LVD current	I_{LVD}	Sleep mode on	-	20	-	uA

4.6 Characteristics of analog modules

4.6.1 Internal clock source characteristics

Table 19. Oscillator characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Calibrated RCH frequency	F_{RCH}	3.3V, -40 to 125°C	15.7*	16.0	16.1	MHz
RCH operating current	I_{RCH}	5.0V, 25°C	-	150	-	uA
RCL frequency	F_{RCL}	1.8 to 5.5V, -40 to 105°C	6	32	50	kHz
RCL operating current	I_{RCL}	-	-	0.3	1.0	uA

Note: RCH is stable at 16MHz from 0 to 125℃, down to 15.8MHz for -10℃, and gradually down to 15.7MHz from -40 to -10℃

4.6.2 ACMP characteristics

Table 20. ACMP characteristics

Parameter		Symbol	Conditions	Minimum	Typical	Maximum	Unit
Typical operating conditions are V_{DD}=3.3V, temperature =25°C, V_{cm} =V_{DD}/2							
Input offset voltage (CPP rising edge)		V_{os}	-	-10	0	10	mV
Input common mode voltage		V_{cm}	Response time<160ns	0	-	V_{DD}	V
Common mode rejection ratio		CMRR	25°C	-	1	-	mV/V
ACMP hysteresis		V_{hyster}	HYS_{min}=0, HYS_{max}=1,	0.4	-	25	mV
Conversion latency		T_{str}	CPDLY 00 to 11, voltage 2.5 to 5V	14	-	2900	ns
Response	rising edge	T_{rt}	V_{DD} as the reference of divided resistor	-	50	100	ns

Parameter		Symbol	Conditions	Minimum	Typical	Maximum	Unit
time	falling edge			-	50	100	ns
Operating current		I_{cmp}	-	-	25	35	uA
CVREF stable time		T_{scvr}	-	-	1	-	us

4.6.3 ADC characteristics

Table 21. ADC characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Typical operating conditions are V_{DD}=3.3V, temperature =25°C, V_{cm} =V_{DD}/2						
Power supply	V_{DDA}	-	2.0	0	5.5	V
Positive reference voltage	V_{ref+}	V_{DDA}>2.5V	2.5	3.3/4	V_{DDA}	V
		V_{DDA}<2.5V		V_{DDA}		V
ADC operating frequency	f_{ADC}	-	-	24	-	MHz
Sampling rate	F_s	V_{DDA}>2.0V, sampling precision>10bits			1.5	MSps
Conversion voltage range	V_{AIN}	-	V_{SSA}	-	V_{ref+}	V
External input impedance	R_{AIN}	-			100	kΩ
Internal sample and hold capacitor	C_{ADC}	-		5		pF
Sampling time	t_{samp}	-	1	-	8	$1/f_{ADC}$
Conversion latency	t_{conv}	-	16	-	48	$1/f_{ADC}$
Internal temperature sensor accuracy	V_{ts}	-40 to 125°C, 3.3V	-	5	-	mV/°C
Operating current	I_{ADC}	1.5MSPS (16MHz), typical	-	1	-	mA

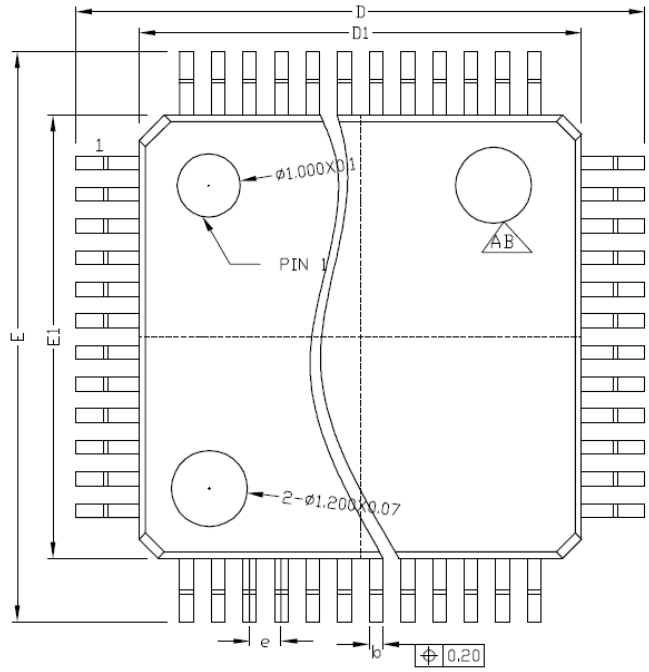
4.6.4 DAC characteristics

Table 22. DAC characteristics

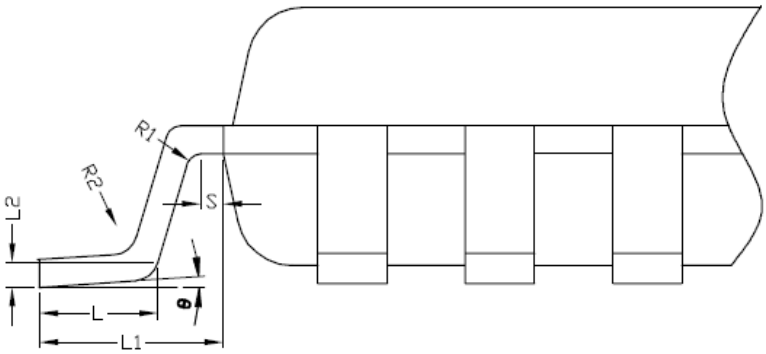
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Typical operating conditions are V_{DD}=3.3V, temperature =25°C, V_{cm} =V_{DD}/2						
Power supply	V_{DDA}	-	2.0	0	5.5	V
Positive reference voltage	V_{ref+}	V_{DDA}>2.5V	2.5	4	V_{DDA}	V
		V_{DDA}<2.5V		V_{DDA}		V
Conversion time	t_{conv}	A correct conversion when small variation in the input code (from code i to i+1 LSB), 8-bit DAC	-	100	-	ns
		A correct conversion when small variation in the input code (from code i to i+1 LSB), 12-bit DAC		2.5		us
Settling time	T_{settle}	3.3V, full scale for an input code transition between the lowest and the highest input codes, 8-bit DAC		0.8		us
		3.3V, full scale for an input code transition between the lowest and the highest input codes, 12-bit DAC		40		us
Output voltage range	V_{AIN}	-	V_{SSA}	-	V_{ref+}	V
Operating current	I_{DAC}	typical	-	150	-	uA

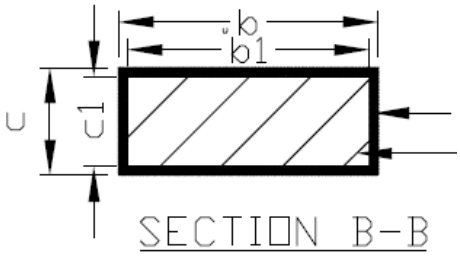
5. Package characteristics

5.1 LQFP32 package outline

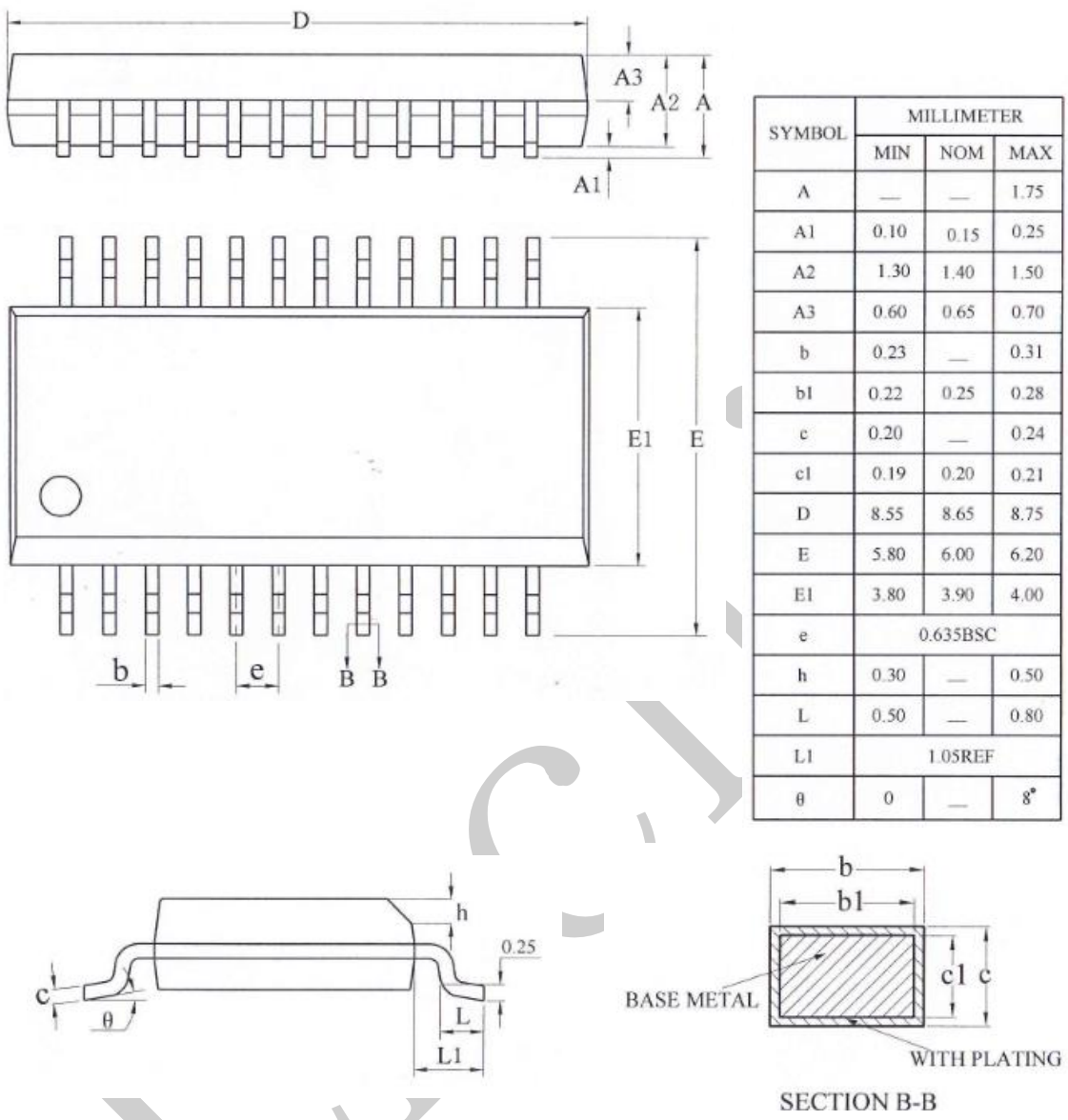


DIM / SYMBOL	LQFP32		
	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	–	0.43
b1	0.31	0.35	0.39
c	0.13	–	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80BSC		
L	0.45	–	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°



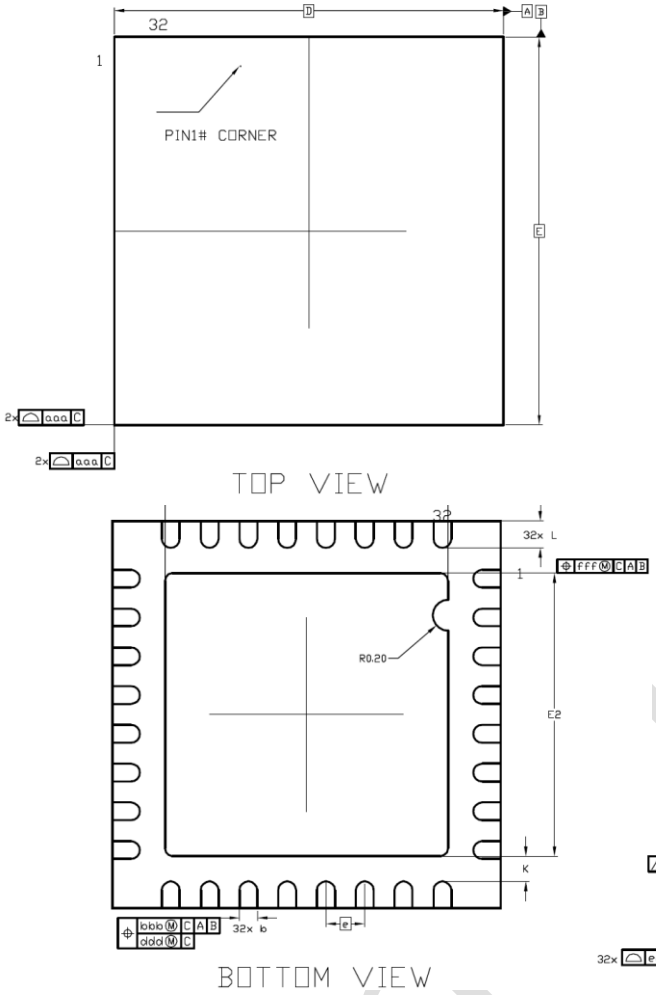


5.2 SSOP24 package outline



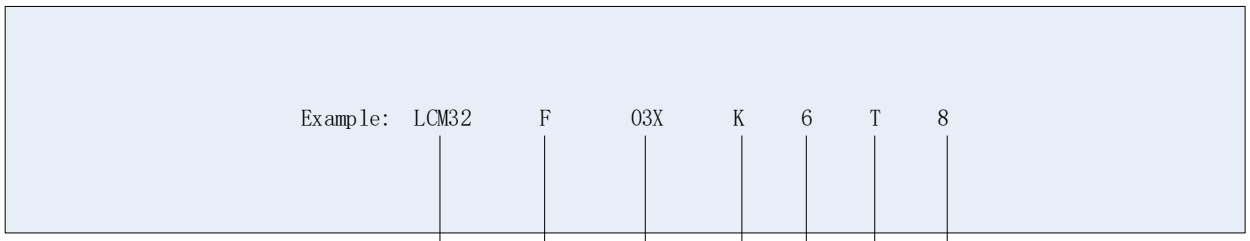
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

5.3 QFN32 package outline



DIM / SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
	0.80	0.85	0.90
A1	0	0.02	0.05
A3	–	0.20 REF	–
b	0.18	0.23	0.28
D	5.00BSC		
E	5.00BSC		
D2	3.55	3.65	3.75
E2	3.55	3.65	3.75
e	0.50BSC		
L	0.30	0.35	0.40
K	–	0.33	–
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

6. Ordering information scheme



Device family

LN32=ARM-based 32-bit microcontroller

Memory type

F: Flash

Product subclass

03x=32-bit M0 processor product

Pin count

H: 24PIN
K: 32PIN
C: 48PIN
R: 64PIN

Flash memory size

4: 16KB
6: 32KB
8: 64KB
B: 128KB

Package

T: LQFP
U: QFN
S: SSOP

Temperature range

6: -20~85℃
7: -40~105℃
8: -40~125℃

7. Revision history

Table 23. Document revision history

Date	Revision	Changes
23-Sep-2021	1.0	Initial release.
9-Nov-2021	1.1	Change operating frequency
9-Dec-2021	1.2	Change A/D conversion rate
13-Dec-2022	1.3	Correction of clerical errors